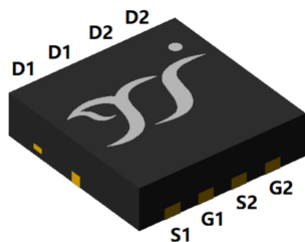
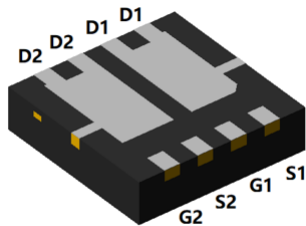


P-Channel Enhancement Mode Field Effect Transistor

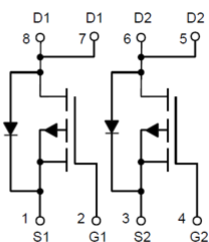


Top View



Bottom View

DFN3333-8L



Product Summary

- V_{DS} -20V
- I_D -30A
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) <19mohm
- $R_{DS(ON)}$ (at $V_{GS} = -2.5V$) <22mohm
- $R_{DS(ON)}$ (at $V_{GS} = -1.8V$) <30mohm

General Description

- Trench Power MV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current	$T_C = 25^\circ C$ @ Steady State	I_D	-30	A
	$T_C = 100^\circ C$ @ Steady State		-19	
	$T_A = 25^\circ C$ @ Steady State		-10	
	$T_A = 100^\circ C$ @ Steady State		-6	
Pulsed Drain Current ^A		I_{DM}	-55	A
Single Pulse Avalanche Energy		E_{AS}	31	mJ
Total Power Dissipation ^B	$T_C = 25^\circ C$ @ Steady State	P_D	21	W
	$T_C = 100^\circ C$ @ Steady State		8.4	
	$T_A = 25^\circ C$ @ Steady State		3	
	$T_A = 100^\circ C$ @ Steady State		1.2	
Thermal Resistance Junction-to-Ambient @ Steady State ^C		$R_{\theta JA}$	42	$^\circ C / W$
Thermal Resistance Junction-to-Case @ Steady State		$R_{\theta JC}$	5.9	$^\circ C / W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQD30P02A	F1	Q30P02	5000	10000	100000	13" reel



YJQD30P02A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =-250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V,V _{GS} =0V,T _C =25℃			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±10V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -4.5V, I _D =-15A		11	19	mΩ
		V _{GS} = -2.5V, I _D =-8A		14	22	
		V _{GS} = -1.8V, I _D =-6.0A		20	30	
Diode Forward Voltage	V _{SD}	I _S =-30A,V _{GS} =0V		-0.8	-1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-10V,V _{GS} =0V,f=1MHZ		2992		pF
Output Capacitance	C _{oss}			330		
Reverse Transfer Capacitance	C _{rss}			272		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V,V _{DS} =-15V,I _D =-9.1A		72.8		nC
Gate Source Charge	Q _{gs}			6.6		
Gate Drain Charge	Q _{gd}			10.1		
Reverse Recovery Charge	Q _{rr}	I _F =-6A, di/dt=100A/us		34		ns
Reverse Recovery Time	t _{rr}			67		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V,V _{DS} =-15V, I _D =-6A, R _{GEN} =2.5Ω		7		
Turn-on Rise Time	t _r			33		
Turn-off Delay Time	t _{D(off)}			130		
Turn-off Fall Time	t _f			132		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. P_d is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

C. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

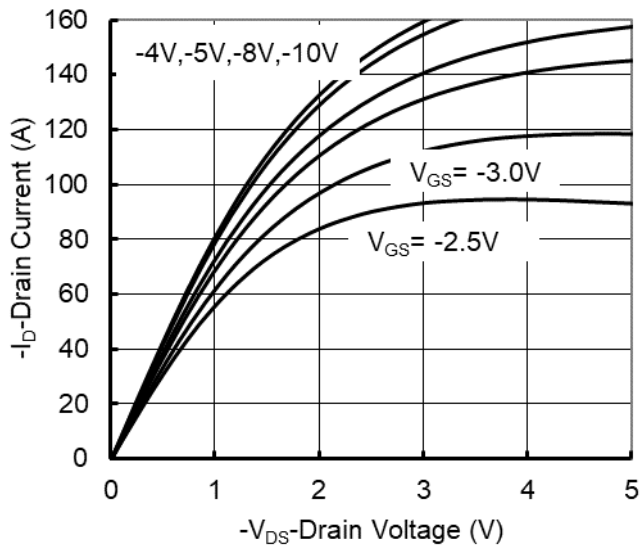


Figure 1. Output Characteristics

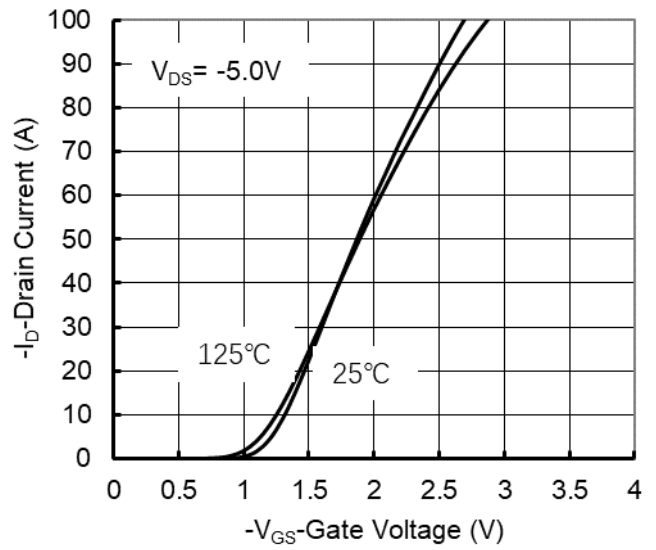


Figure 2. Transfer Characteristics

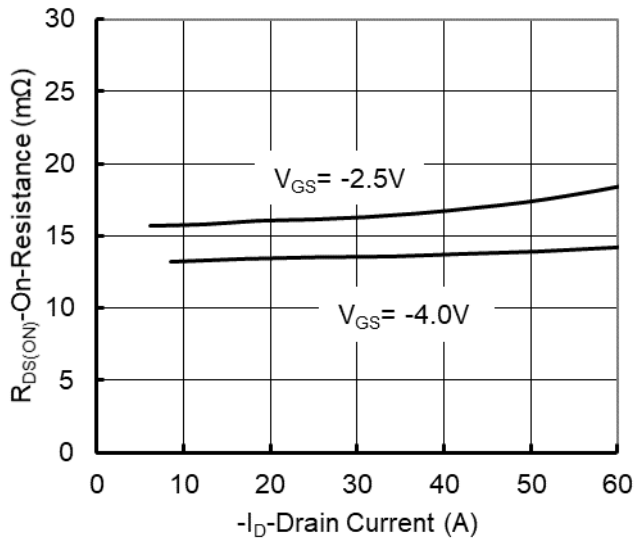


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

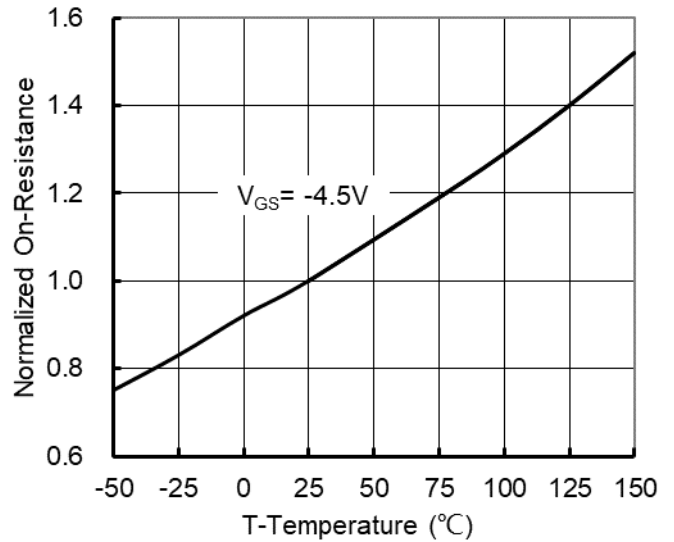


Figure 4. On-Resistance vs. Junction Temperature

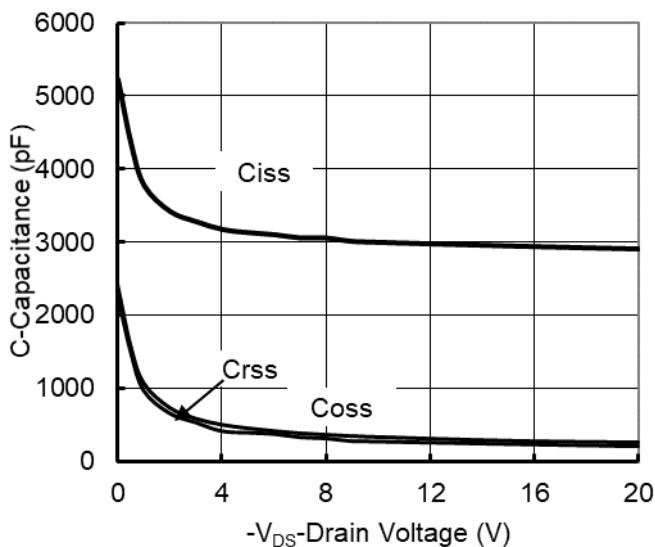


Figure 5. Capacitance Characteristics

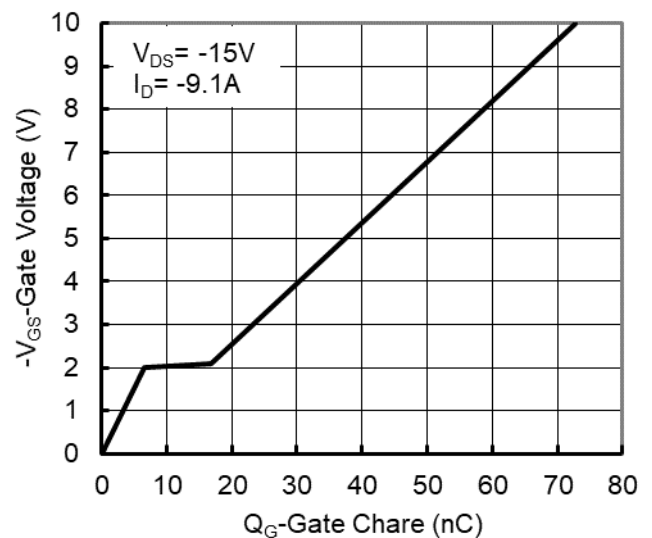


Figure 6. Gate Charge



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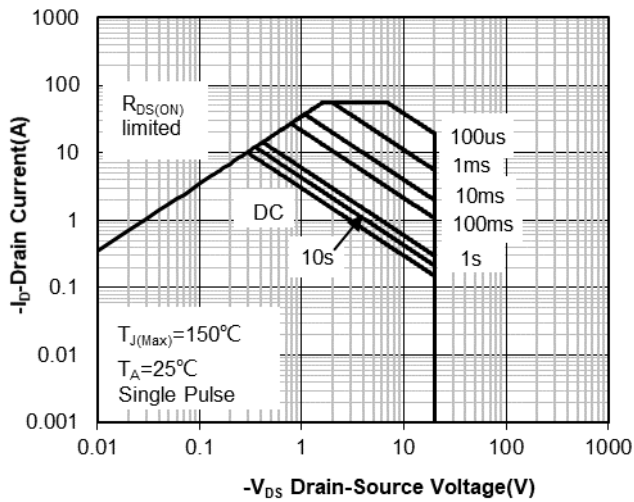


Figure 7. Safe Operation Area

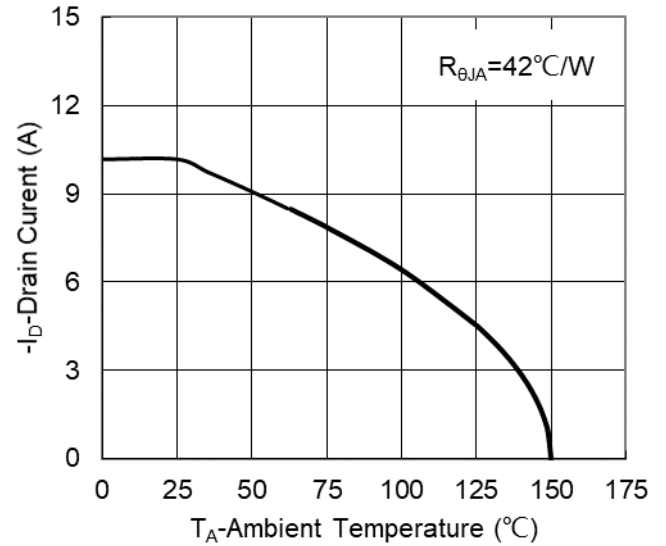


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

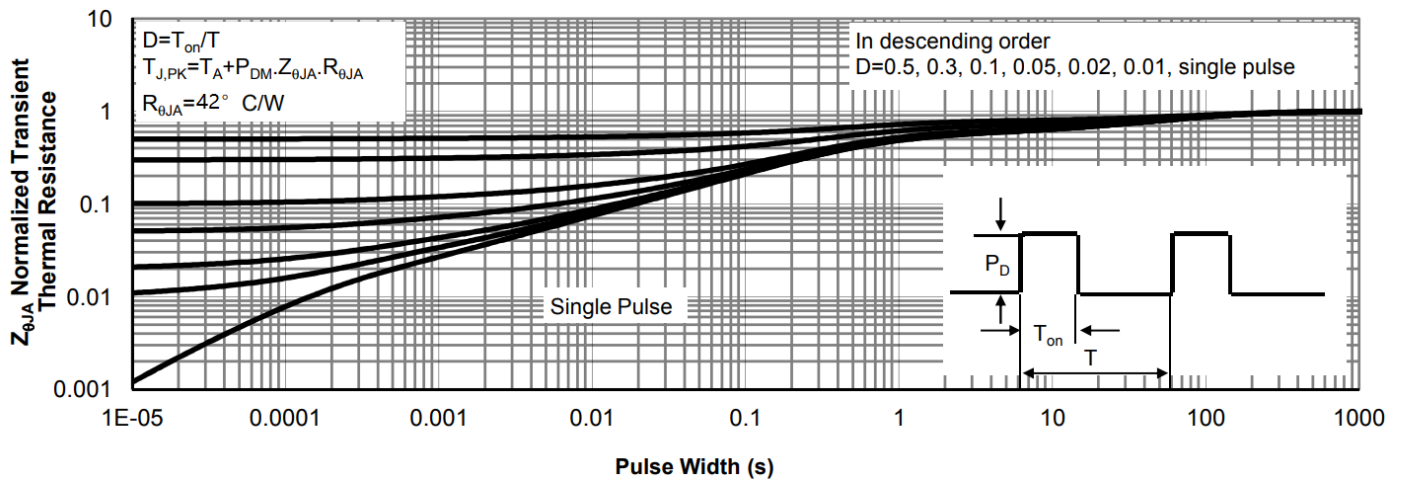
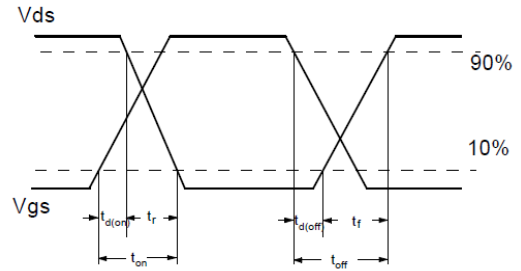
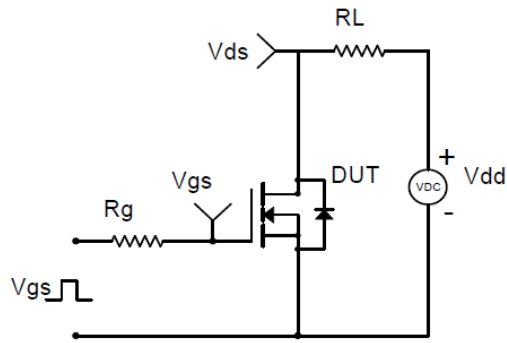
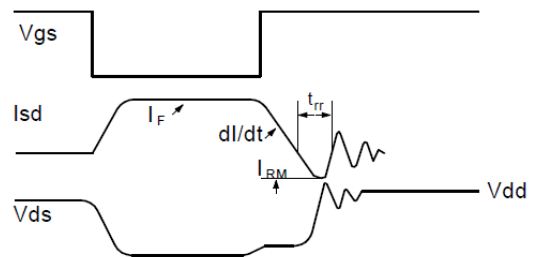
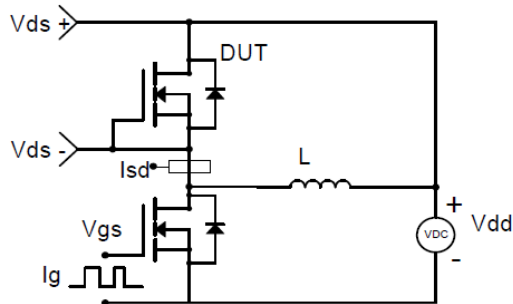


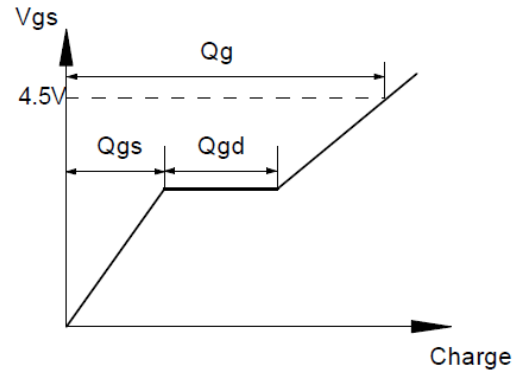
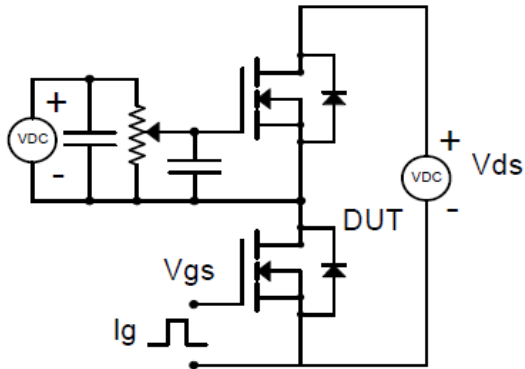
Figure 9. Normalized Maximum Transient Thermal Impedance



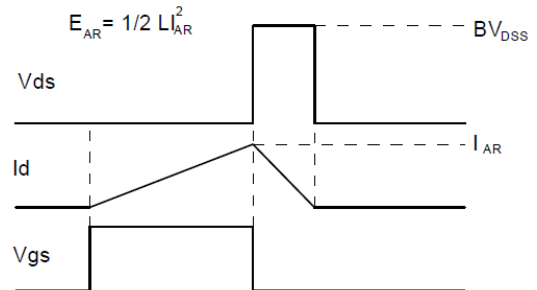
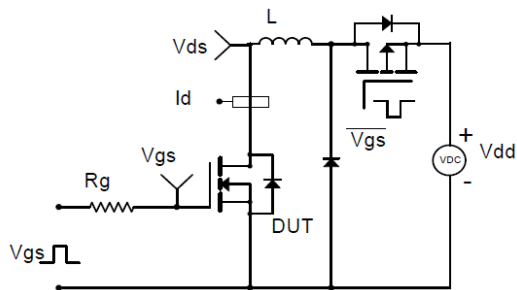
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

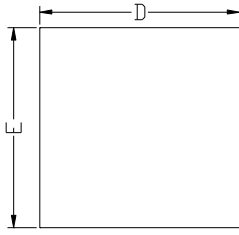


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

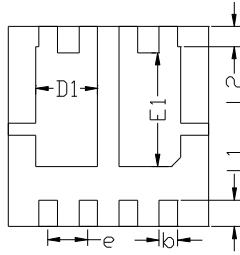


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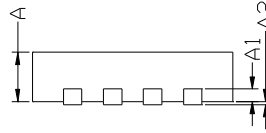
■ DFN3333-8L Package information



Top View
正面视图

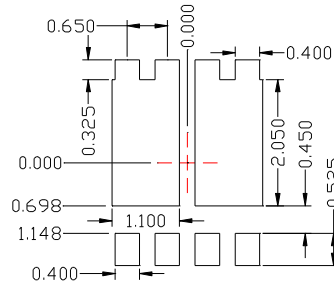


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.90	1.00	1.10
E1	1.75	1.85	1.95
L1	0.325	0.425	0.525
L2	0.325 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.



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